| | |
|---|---|
| **Course name** | **ECE 55801 Advanced Systems on a Chip (SoC) Designs for Image Processing using FPGAs (ECE 595)** |
| **Credit and contact hours** | (3 cr.) Class 3 |
| **Course coordinator's name** | Lauren Christopher |
| **Textbook** | Pedroni, Volnei A., *Circuit Design and Simulation with VHDL*, 2nd Ed., MIT Press, ISBN-10: 0262014335 \| ISBN-13: 978-0262014335 |
| **Course information** | **2014-16 IUPUI Campus Bulletin description:**<br>ECE 55801 Advanced Systems on a Chip (SOC) Designs for Image Processing using FPGAs. Credit 3. P: ECE 42100 and ECE 30100; or Graduate Standing. This class covers advanced concepts in using Field Programmable Gate Arrays (FPGAs) designed with an HDL (VHDL for example: Very High Speed IC Hardware Description Language). The students will learn complex interface design, advanced hardware and embedded system design and parallel processing. Projects and lessons will focus on applications in Digital Imaging Systems. Lecture and projects covering topics including: VHDL mapped to FPGA for state machine design, hardware and software VGA control, image filtering, data transfer to PCI bus, and embedded controller integration.<br><br>**Prerequisites/ Co-Requisite**<br>P: ECE 42100 and ECE 30100; or Graduate Standing<br><br>**Required, Elective, or Selected Elective:**<br>EE Elective, CE Elective |
| **Goals for the course** | Upon successful completion of the course, students should be able to<br>1. Design and simulate complex systems for FPGA using and HDL. [a, b, c]<br>2. Map system designs to FPGA hardware. [a, b, c, e, k]<br>3. Develop FPGA system with embedded software. [a, b, c, e, k]<br>4. Apply FPGA design to image processing problems. [a, b, c, e]<br>5. Use a team to develop a novel design of an imaging system on the FPGA. [c, d, k] |
| **List of topics to be covered** | 1. Course Instructions, introduction and review (2 classes)<br>2. System Design with VHDL (3 classes)<br>3. Extended and Advanced Design with FPGAs (3 classes)<br>4. Image Processing with FPGA (4 classes)<br>5. Student Final Team Project (4 classes)<br>6. Quizzes and Exams (2-4 classes)<br>**Laboratory Projects:** |

| | |
|---|---|
| | The course will include homework and Xilinx board lab design projects. This will involve programming in VHDL or Verilog and the use of simulation tools and hands-on experiments with FPGA development boards. The students will submit short project reports for the individual small projects. Final Project will be a team effort which requires the students to submit a written project report and give a presentation. |
| **Syllabi approved by** | Lauren Christopher |
| **Date of approval** | 04/16/2016 |